TypeC User define register

DP apb register base address: 0x6000\_0000

DP apb register address range: 0x6000\_0000 ~ 0x600f\_ffff

DP sapb register base address: 0x6010\_0000

DP sapb register address range: 0x6010\_0000 ~ 0x601f\_ffff

DP capb register base address: 0x6020\_0000

DP capb register address range: 0x6020\_0000 ~ 0x602f\_ffff

USB register base address: 0x6030\_0000

USB register address range: 0x6030\_0000 ~ 0x6033\_ffff

TCPD register base address: 0x6034\_0000

TCPD register address range: 0x6034\_0000 ~ 0x6037\_ffff

Common PHY register base address: 0x6038\_0000

Common PHY register address range: 0x6038\_0000 ~ 0x603b\_ffff

TypeC user define register base address: 0x603c\_0000

TypeC user define register address range: 0x603c\_0000 ~ 0x603f\_ffff

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Register Name | Offset | Type | Reset Value | Field |
| register\_00 | 0x0000 | WR | 32’h0 | xtensa related register. bit[0]-xten\_sel:PHY register arbiter between Xtensa FW and PHY bit[1]-apb\_addr\_sel:apb address decoder mux select signal |
| typec\_ctrl0 | 0x0004 | WR | 32’h0552\_2000 | bit[0]-ucpu\_jtag\_en: cpu(xtensa) jtag enable bit[1]-ucpu\_jtag\_sel: dp/tcpd xtensa jtag select; Only active when bit[0](ucpu\_jtag\_en) asserted. bit[2]-dp\_vif\_dis: dp source frame disable signal bit[3]-source\_crypto\_dis: dp crypto disable signal bit[5:4]-strap:static strap pin control from system to  configure TCPC default mode; not advertise(00b)/DFP(01b)/UFP(10b)/DRP(11b) bit[8:6]-mode\_strap:default mode to be activated after POR; both modes are off(000b)/controller initially configured as Host(010)/as Device(100)/other-RSVD  bit[9]-psm\_clk\_ext\_select: 1’b1-external PSM clock selected and ‘phy\_ext\_psm\_clk’ will be used as PSM clock for internal operation; 1’b0-PHY generated PSM clock selected for internal operation bit[10]-use\_ext\_phy\_reset: selects phy\_reset\_n source: 1’b0-internal phy\_reset\_n signal is controlled by system SW using USBSS-DRD TYPEC\_CFG register; 1’b1-internal phy\_reset\_n is sourced from USBSS-DRD primary input-phy\_reset\_n bit[11]-utmi\_clk\_sel:utmi clock select. 1’b0-60MHz;1’b1-30MHz bit[18:12]-RSVD bit[19]-dptx\_xtensa\_ls\_reg: memory ls value bit[20]-dptx\_xtensa\_ls\_sel: memory ls source select. LS=ls\_sel?ls\_reg:!en; bit[21]-dptx\_ls\_reg: bit[22]-dptx\_ls\_sel: bit[23]-usb\_ls\_reg: bit[24]-usb\_ls\_sel: bit[25]-tcpd\_xtensa\_ls\_reg: bit[26]-tcpd\_xtensa\_ls\_sel: bit[27]-i2s\_src\_sel: I2S audio source select. 1’b0-Original; 1’b1-HDMI bit[28]-usbdrd\_buf\_ds: bit[29]-usbdrd\_buf\_sd: bit[30]-tcpd\_xtensa\_dram\_ds: bit[31]-tcpd\_xtensa\_dram\_sd: |
| typec\_ctrl1 | 0x0008 | WR | 32’h0 | bit[0]-xhci\_main\_power\_on\_valid: status from system to indicate to xhci that MAIN power is active(should be driven in AUX domain) bit[1]-xhci\_main\_power\_off\_req: request from system to prepare xhci for MAIN power removal bit[2]-aux\_app\_clk\_125\_valid: status from system indicating that app\_clk\_predft is running and at correct frequency  bit[3]-lpm\_clk\_valid: status from system indicating that lpm\_clk\_predft is running and at correct frequency bit[4]-phy\_refclk\_valid: reference clock is stable (+/-300ppm)  bit[5]-phy\_refclk\_1pct\_valid:reference clock is stable (+/-1%) bit[6]-mdctrl\_clk\_sel: OTG logic clock select  bit[7]-usbdev\_main\_power\_off\_req:request from system to prepare USBSS-DEV for USBSS-DEV MAIN power removal  bit[8]-usbdev\_main\_power\_on\_valid:status from system power manager that USBSS-DEV MAIN power is stable  bit[9]-usbdev\_power\_off\_req: request from system to prepare USBSS-DEV for USBSS-DEV AUX power removal  bit[10]-usbdev\_power\_on\_valid: status from system power manager that USBSS-DEV for USBSS-DEV AUX power is stable  bit[11]-xhci\_power\_off\_req: request from system to prepare xhci for xhci AUX power removal  bit[12]-xhci\_power\_on\_valid: status from system power manager that xhci power is stable  bit[13]-xhc\_d0\_req:external D0 state request  bit[14]-ltm\_host\_req\_halt:Backpressure LTM Host Message request  bit[15]-host\_system\_err:The signal indicates that there is a very serious error detected such that we should turn off run\_stop bit  bit[20:16]-xhci\_debug\_sel:xhci debug mux select signal  bit[21]-wakeup:  bit[22]-usbrst\_dis:usb pwrup reset disable signal  bit[23]-tcpdrst\_dis:tcpd pwrup reset disable signal  bit[24]-TCPD\_OCDHaltOnReset value:  TCPD\_OCDHaltOnReset=ucpu\_jtag\_en&&!ucpu\_jtag\_sel?typec\_ctrl1[24]:0;  bit[26:25]-bpc\_sel:video color depth sel(2’b00-8bpc; 2’b01-10bpc; others-RSVD)  bit[27]-alert\_n\_pol:alert\_n polarity  alert\_n\_final = alert\_n\_pol ? alert\_n : ~alert\_n  bit[28]-vir\_clk\_en: no used clock enable signal(spdif, trng clock etc.); default disable bit[29]-source\_spdif\_din: Audio SPDIF data in; only for synthesis(can be omitted) bit[30]-debug\_access\_en: access dp debug area enable; originally equals to ‘source\_secure\_mode’ in source code  bit[31]-RSVD |
| typec\_ctrl2 | 0x000c | WR | 32’h0 | bit[0]-dptx\_xtensa\_dram\_ds: bit[1]-dptx\_xtensa\_dram\_sd: bit[2]-dptx\_xtensa\_iram\_ds: bit[3]-dptx\_xtensa\_iram\_sd:[‘it[4]-dptx\_vid\_mem\_ds: bit[5]-dptx\_vid\_mem\_sd: bit[6]-dptx\_aud\_mem\_ds: bit[7]-dptx\_aud\_mem\_sd: bit[8]-dptx\_sdp\_mem\_ds: bit[9]-dptx\_sdp\_mem\_sd: bit[10]-tcpd\_xtensa\_iram\_ds: bit[11]-tcpd\_xtensa\_iram\_sd: bit[12]-usbdrd\_bw\_ram1\_ds: bit[13]-usbdrd\_bw\_ram1\_sd: bit[14]-usbdrd\_bw\_ram2\_ds: bit[15]-usbdrd\_bw\_ram2\_sd: bit[16]-usbdrd\_tte\_ram\_ds: bit[17]-usbdrd\_tte\_ram\_sd: bit[18]-usbdrd\_prot\_data\_asyn\_xbuf\_ds: bit[19]-usbdrd\_prot\_data\_asyn\_xbuf\_sd: bit[20]-usbdrd\_prot\_data\_per\_xbuf\_ds: bit[21]-usbdrd\_prot\_data\_per\_xbuf\_sd: bit[22]-usbdrd\_hs\_prot\_data\_asyn\_xbuf\_ds: bit[23]-usbdrd\_hs\_prot\_data\_asyn\_xbuf\_sd: bit[24]-usbdrd\_hs\_prot\_data\_per\_xbuf\_ds: bit[25]-usbdrd\_hs\_prot\_data\_per\_xbuf\_sd: bit[26]-usbdrd\_hs\_prot\_data\_rbuf\_ds: bit[27]-usbdrd\_hs\_prot\_data\_rbuf\_sd: bit[28]-usbdrd\_split\_prot\_data\_asyn\_xbuf\_ds: bit[29]-usbdrd\_split\_prot\_data\_asyn\_xbuf\_sd: bit[30]-usbdrd\_split\_prot\_data\_per\_xbuf\_ds: bit[31]-usbdrd\_split\_prot\_data\_per\_xbuf\_sd: |
| typec\_ctrl3 | 0x0010 | WR | 32’h0 | bit[0]-usbdrd\_split\_prot\_data\_rbuf\_ds: bit[1]-usbdrd\_split\_prot\_data\_rbuf\_sd: bit[2]-usbdrd\_cpl\_collect\_ds: bit[3]-usbdrd\_cpl\_collect\_sd: bit[4]-usbdrd\_dbgp\_bulkin\_ram\_ds: bit[5]-usbdrd\_dbgp\_bulkin\_ram\_sd: bit[6]-usbdrd\_dbgp\_bulkout\_ram\_ds: bit[7]-usbdrd\_dbgp\_bulkout\_ram\_sd: bit[8]-usbdrd\_dbgp\_strfifo\_ram\_ds: bit[9]-usbdrd\_dbgp\_strfifo\_ram\_sd: bit[10]-usbdrd\_idma\_addr\_ram\_ds: bit[11]-usbdrd\_idma\_addr\_ram\_sd: bit[12]-usbdrd\_prot\_hdr\_rbuf\_ds: bit[13]-usbdrd\_prot\_hdr\_rbuf\_sd: bit[14]-usbdrd\_prot\_data\_rbuf\_ds: bit[15]-usbdrd\_prot\_data\_rbuf\_sd: bit[16]-usbdrd\_tte\_ram\_ds: bit[17]-usbdrd\_tte\_ram\_sd: bit[18]-usbdrd\_rd\_cmd\_ds: bit[19]-usbdrd\_rd\_cmd\_sd: bit[20]-usbdrd\_wr\_cmd\_ds: bit[21]-usbdrd\_wr\_cmd\_sd: bit[22]-usbdrd\_wr\_data\_ds: bit[23]-usbdrd\_wr\_data\_sd: bit[24]-usbdrd\_slot\_cntx\_ds: bit[25]-usbdrd\_slot\_cntx\_sd: bit[26]-usbdrd\_sch\_cntx\_ds: bit[27]-usbdrd\_sch\_cntx\_sd: bit[28]-usbdrd\_trm\_cntx\_ds: bit[29]-usbdrd\_trm\_cntx\_sd: bit[30]-usbdrd\_dma\_cntx\_ds: bit[31]-usbdrd\_dma\_cntx\_sd: |
| typec\_ctrl4 | 0x0014 | WR | 32’h0 | bit[0]-tcpd\_vbus\_overvoltage\_n:  tcpd\_vbus\_overvoltage\_n = !typec\_ctrl4[0] bit[10:1]-tcpd\_vbus\_voltage: 10bits voltage selected if needed bit[11]-axi\_cache\_sel:  awcache = axi\_cache\_sel ? awcache\_reg : awcache\_org;  arcache = axi\_cache\_sel ? arcache\_reg : arcache\_org; bit[15:12]-awcache\_reg bit[19:16]-arcache\_reg |
| typec\_ctrl5 | 0x0018 | WR | 32’h0 | RSVD |
| typec\_ctrl6 | 0x001c | WR | 32’h0 | DP Freerun pattern related register bit[15:0]-hwidth: horizontal active pixels bit[31:16]-htotal: horizontal total pixels |
| typec\_ctrl7 | 0x0020 | WR | 32’h0 | DP Freerun pattern related register bit[15:0]-vheight: vertical active lines bit[31:16]-vtotal: vertcal total lines |
| typec\_ctrl8 | 0x0024 | WR | 32’h0 | DP Freerun pattern related register bit[15:0]-hstart: hsync+hbp bit[31:16]-vstart: vsync+vbp |
| typec\_ctrl9 | 0x0028 | WR | 32’h0 | DP Freerun pattern related register bit[15:0]-hsw: horizontal sync width bit[31:16]-vsw: vertical sync width |
| typec\_ctrla | 0x002c | WR | 32’h0 | DP Freerun pattern related register bit[5:0]-patgen\_ctrl: freerun pattern mux signals bit[6]-fr\_sel: dp source select from freerun pattern  bit[31:7]-RSVD |
| register\_0c | 0x0030 | WR | 32’h0 | RSVD |
| register\_0d | 0x0034 | WR | 32’h0 | RSVD |
| register\_0e | 0x0038 | WR | 32’h0 | RSVD |
| register\_0f | 0x003c | WR | 32’h0 | RSVD |
| typec\_status0 | 0x0040 | RO | 32’h0 | bit[31:24]-8’h00 bit[23]-tcpd\_vbus\_voltage\_en bit[22]-tcpd\_vbus\_overvoltage\_en  bit[21]-tcpd\_outs\_to\_hiz  bit[20]-tcpd\_dbg\_acc\_conn\_n  bit[19]-tcpd\_audio\_acc\_conn\_n  bit[18]-tcpd\_act\_cable\_conn  bit[17:16]-tcpd\_mux\_ctrl:Type-C mode selection: 00b-No connection; 01b:USB3.1; 10b:DP 4lanes; 11b-USB3.1+DP lanes 0 & 1  bit[15]-tcpd\_conn\_present  bit[14]-tcpd\_conn\_orientation  bit[13:2]-lowest\_belt: Lowest Belt seen by Host  bit[1]-source\_sirq: dp sapb interrupt  bit[0]-source\_pirq: dp apb interrupt |
| typec\_status1 | 0x0044 | RO | 32’h0 | bit[31:21]-11’h00 bit[20]-ltm\_host\_req  bit[19]-xhc\_d0\_ack  bit[18]-xhci\_power\_on\_ready  bit[17]-xhci\_power\_on\_req  bit[16]-xhci\_power\_off\_ready  bit[15]-xhci\_power\_off\_ack  bit[14]-usbdev\_power\_on\_ready  bit[13]-usbdev\_power\_on\_req  bit[12]-usbdev\_power\_off\_ready  bit[11]-usbdev\_power\_off\_ack  bit[10]-usbdev\_power\_on\_ready  bit[9]-usbdev\_main\_power\_on\_req  bit[8]-usbdev\_main\_power\_off\_ready  bit[7]-usbdev\_main\_power\_off\_ack  bit[6]-mdctrl\_clk\_status  bit[5]-phy\_refclk\_req  bit[4]-lpm\_clk\_req  bit[3]-aux\_app\_clk125\_req  bit[2]-xhci\_main\_power\_off\_ack  bit[1]-xhci\_main\_power\_on\_ready  bit[0]-xhci\_main\_power\_on\_req |
| typec\_status2 | 0x0048 | RO | 32’h0 | bit[31]-1’b0; bit[30:0]-xhci\_debug\_link\_state |
| typec\_status3 | 0x004c | RO | 32’h0 | bit[31:0]-xhci\_debug\_bus |